



Veljko Milutinović

VLSI for SuperComputing: From Applications and Algorithms to Masks and Chips

World Top Foundries in VLSI for SuperComputing

- #1?



World Top Foundries in VLSI for SuperComputing

- #1? Qualcomm

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- #2?



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- #3? Mubadala (AMD, ...)



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Who works here?





The Holistic Foundry (R&DFab) in VLSI for SuperComputing

- Phase#1: From Applications to Algorithms
Phase#2: From Algorithms to Masks
Phase#3: From Masks to Chips



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- Phase#1: From Applications to Algorithms
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Phase#3: From Masks to Chips
- Verification is crucial
in each one of these phases,
and related teaching is done in coop with ELSYS!



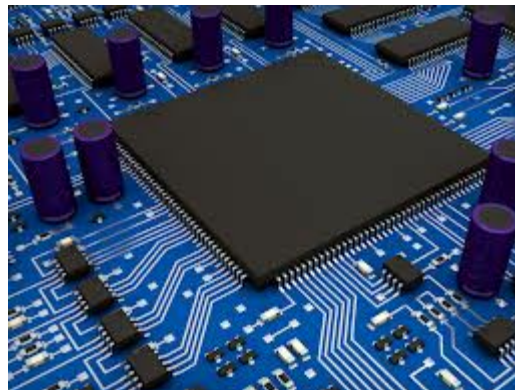
The Holistic Foundry (R&DFab) in VLSI for SuperComputing

- Phase#1: From Applications to Algorithms
Phase#2: From Algorithms to Masks
Phase#3: From Masks to Chips
- Verification is crucial
in each one of these phases,
and related teaching is done in coop with ELSYS!
- Management issues of importance for an R&DFab
are covered in the accompanying course: IR4USP
(including 12 related homework assignments)!

Contents:

From Algorithms to Masks

- Part#1: VLSI for ControlFlow SuperComputing
- Part#2: VLSI for DataFlow SuperComputing
- Part#3: VLSI for WirelessFlow SuperComputing





VLSI for ControlFlow SuperComputing

ManyCore Systems:

- Enabler Technology: VHDL vs Verilog (0.5 weeks)
- Design and Programming of a 200MHz RISC Microprocessor (2.5 weeks) + HW#1


MultiCore Systems:


- Enabler Technology: Verification by Elsys (2 weeks) + Lab#1
- Design of MicroProcessor and MultiMicroProcessor Systems by Wiley (1 week)

SURVIVING THE DESIGN OF A
200 MHz RISC
MICROPROCESSOR
LESSONS LEARNED



Veljko Milutinović
Foreword by Michael Flynn

 Cambridge University Press

 THE INSTITUTE OF ELECTRICAL AND
ELECTRONICS ENGINEERS

SURVIVING THE DESIGN OF
MICROPROCESSOR
AND
MULTIMICROPROCESSOR
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LESSONS LEARNED



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Wiley Series on Parallel and Distributed Computing
Albert Y. Zomaya, Series Editor



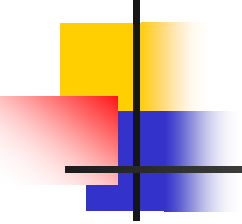
VLSI for DataFlow SuperComputing

FineGrain DataFlow:

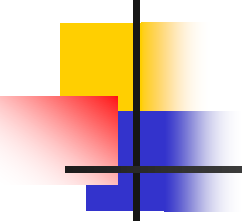
- Enabler Technology: Altera vs Xilinx (0.5 weeks)
- Design and Programming of the 200MHz Maxeler Machine (3.5 weeks) + HW#2

SystolicArray DataFlow:

- Enabler Technology: Systolic Array Architectures (0.5 weeks)
- Design of DARPA Systolic Architectures (0.5 weeks) + Lab#2

- 
-
- **Advances in Computer Architecture**
(North Holland)
by Veljko M. Milutinovic
with a contribution from John Hennessy



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- **High-Level Language Computer Architecture**
(Elsevier Computer Science Press)
by Veljko M. Milutinovic
with a contribution from Michael Flynn





VLSI for WirelessFlow SuperComputing

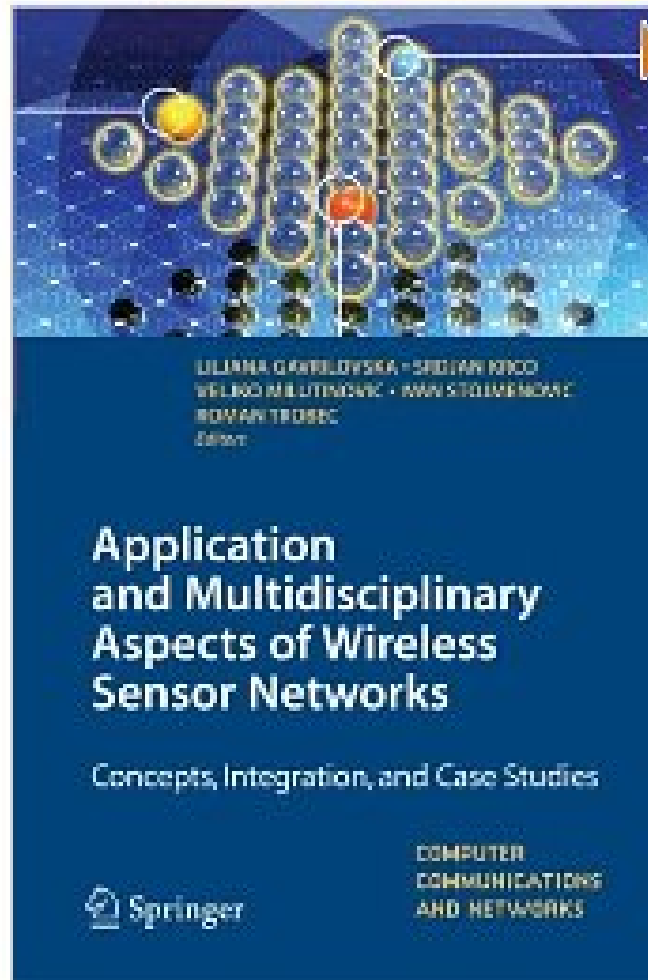
WSNs: Part#1

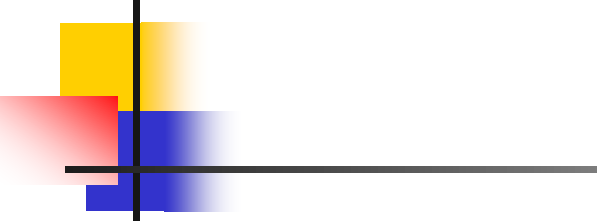
- Hardware (0.25 weeks)
- Software (0.25 weeks)

WSNs: Part#2

- Systems (SUN+Slimmer) (0.25 weeks)
- Applications (UbiComputing@WSN+DataMining@WSN) (0.25 weeks)

Click to **LOOK INSIDE!**






Goran Rakocevic · Tijana Djukic
Nenad Filipovic · Veljko Milutinovic
Editors

Computational Medicine in Data Mining and Modeling

opt.html

 Springer



VLSI for QuantumMechanical SuperComputing

Basics:

- Hardware (0 weeks)
- Software (0 weeks)

Advances:

- Systems (0 weeks)
- Applications (0 weeks)

Optional class projects for extra points!



European Projects

ESF:

- RoMoL: Riding on Moore's Law (0 weeks)
- HiPeac: Parallel Programming Models (0 weeks)

FP7/H20:

- FP7: ProSense (0 weeks)
- FP7: BalCon (0 weeks)



Example Algorithms for Practical Implementations

Engineering:

- Computer Engineering (0 weeks)
- Financial Engineering (0 weeks)

Science:

- Physical Chemistry (0 weeks)
- Computer Science (0 weeks)

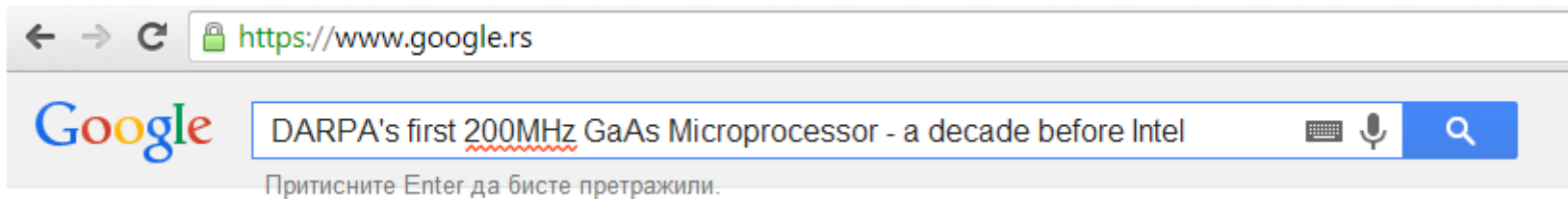


SOME PREVIOUS OFFERINGS OF THIS TECH COURSE

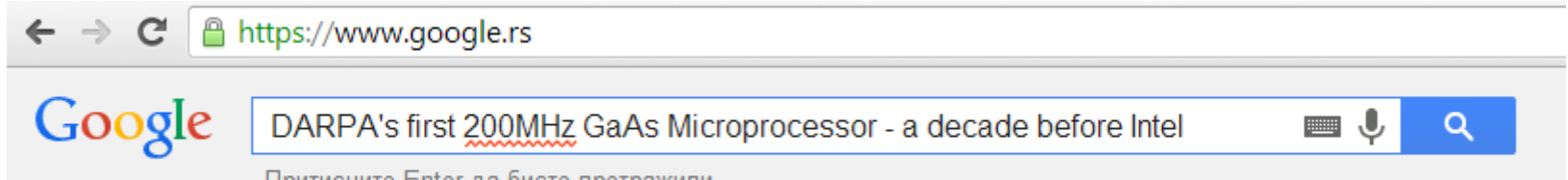
- Purdue
- Stanford
- MIT
- Barcelona
- Siena
- Ljubljana

Previous offerings of the related MGMT course: Purdue, Dartmouth, HarvardCNY, Barcelona, Pisa, Ljubljana

BOTTOM LINE: BRINGING ADVANCED INDUSTRIAL EXPERIENCE INTO THE CLASSROOM



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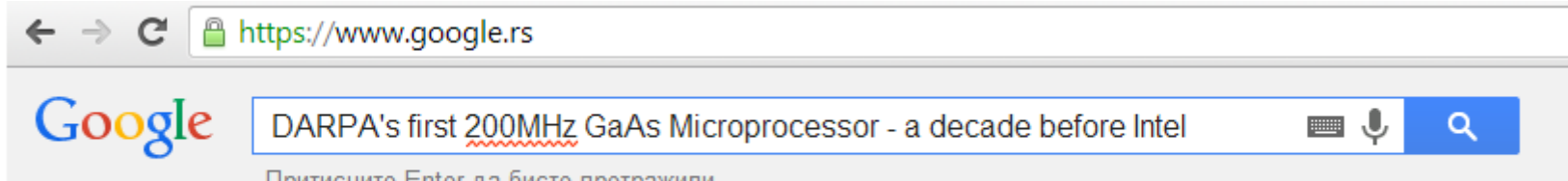


[Milutinovic, Veljko \(Serbia\)](#)

[www.balcon-project.eu](#) > ... > [Serbia](#) ▾ Преведи ову страницу

... the first GaAs microprocessor in the world, agency DARPA project Star Wars, ...
project has realized processor speed of 200MHz about a decade before Intel, ...

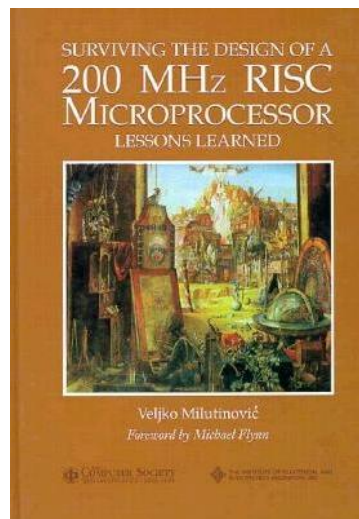
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BOTTOM LINE: BRINGING ADVANCED INDUSTRIAL EXPERIENCE INTO THE CLASSROOM (2)

Google

MAXELER - today's fastest dataflow supercomputer for oil and gas industry



Притисните Enter да бисте претражили.

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[HPCwire: Maxeler Launches MPC-X Series Dataflow Engines](#)

www.hpcwire.com/.../maxeler_launches_mpc-x_... ▼ Преведи ову страницу

21.03.2012. - **Market Watch**; Events ... "At **Maxeler** we are excited to offer the **fastest** computers on the planet ... in **Oil and Gas** exploration and in a range of other application areas. ...

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Veljko Milutinovic

Dr. Veljko Milutinovic is a professor at the School of Electrical Engineering, University of Belgrade, Serbia. During the 80's, for about a decade, he was on the faculty of Purdue University in the U.S.A, where he co-authored the architecture and design of the world's first DARPA GaAs microprocessor. During the 90's, after returning to Serbia, he took part in teaching and research at a number of major EU schools. He also delivered lectures at Stanford and MIT, and has about 20 books published by leading publishers in the U.S.A. Dr. Milutinovic is a Fellow of the IEEE and a Member of Academia Europaea.

BOTTOM LINE: BRINGING ADVANCED INDUSTRIAL EXPERIENCE INTO THE CLASSROOM (3)



Google

Ericsson - the ProSense project



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Ericsson - the ProSense project



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[PPT Authors - kondor.etf.rs](#)

home.etf.rs/~vm/Belgrade%20overview.ppt ▾ Преведи ову страницу

ProSense. 3 /30. **ProSense.** Project Team. Director for EU: Dr. Srđan Krčo, **Ericsson**, Ireland. Director for Serbia: Prof. Dr. Veljko Milutinović, UB. Team members.

BOTTOM LINE: BRINGING ADVANCED INDUSTRIAL EXPERIENCE INTO THE CLASSROOM (3)



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Wireless Sensor Networks: ApplicationDesign and DataMining



